Cu electroplating in advanced packaging

March 12 2019

Richard Hollman PhD
Principal Process Engineer

- Advancements in package technology
- The role of electroplating
- Examples: 4 challenging structures

Old paradigm: clear functional separation

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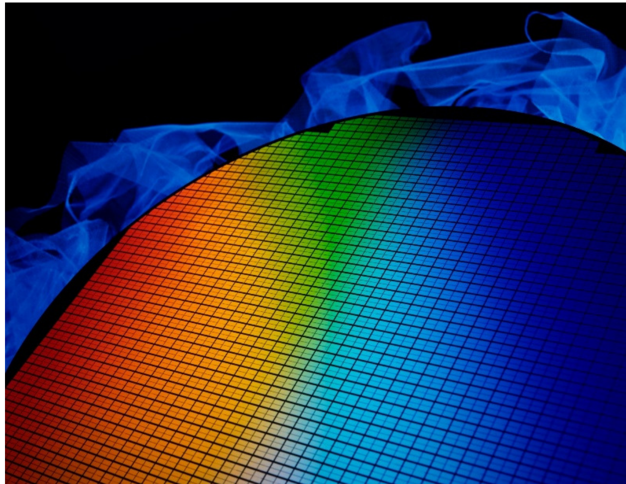
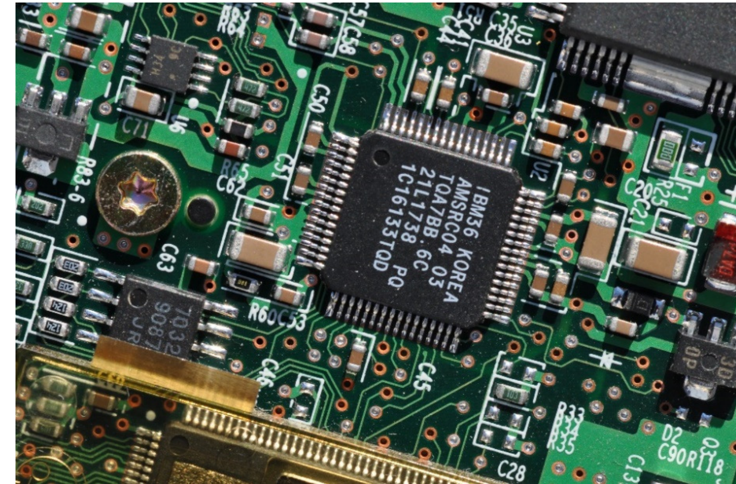




IC:

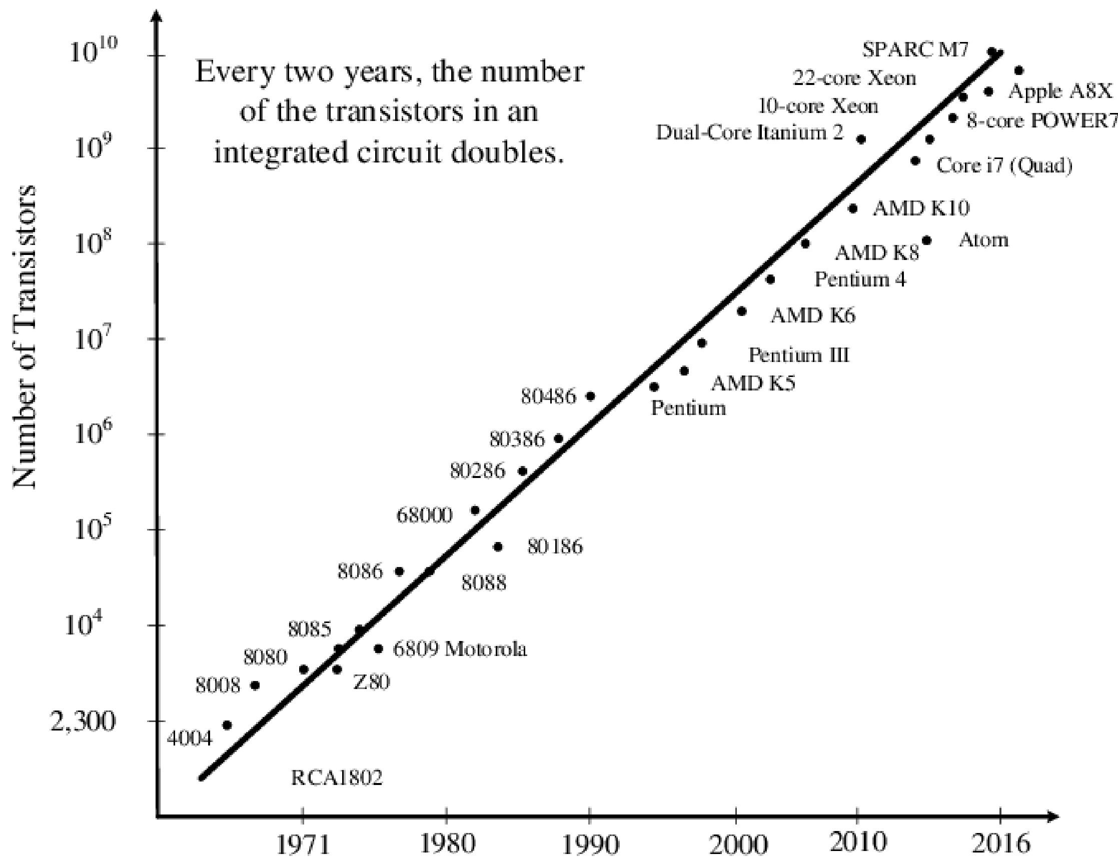
- Primary location for performance improvement
- Primary location for increasing integration

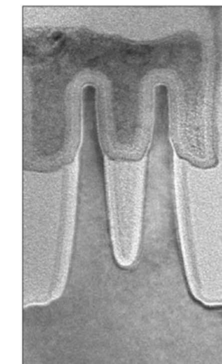
Board:

- Connection of heterogeneous components
    - IC's
    - Passives
    - Switches, indicators
    - Peripherals

Moore's Law on the wafer side

First transistor
1947 Bell Labs




14 nm 2nd Generation
Tri-gate Transistor

The longevity of the PWB concept

Between the IC and the board: the Package

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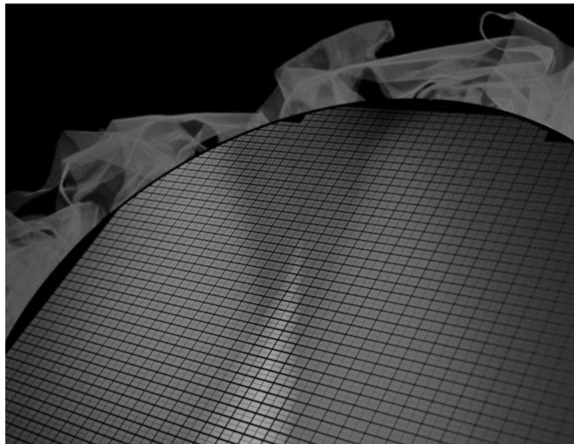

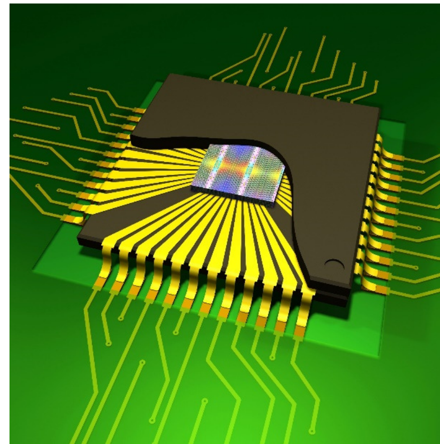

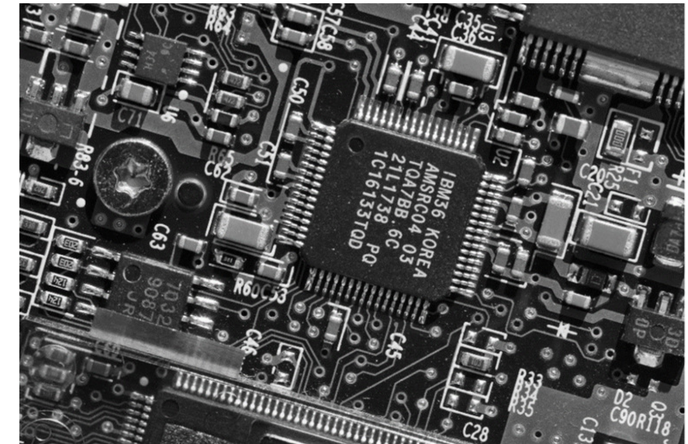

IC:
- Primary location for performance improvement
- Primary location for increasing integration

Package (old paradigm):
- Mechanical protection for IC
- Transparent 1:1 interface between chip I/O and board

Board:
- Connection of heterogeneous components
  - IC’s
  - Passives
  - Switches, indicators
  - Peripherals

New paradigm: package takes on aspects of IC and board

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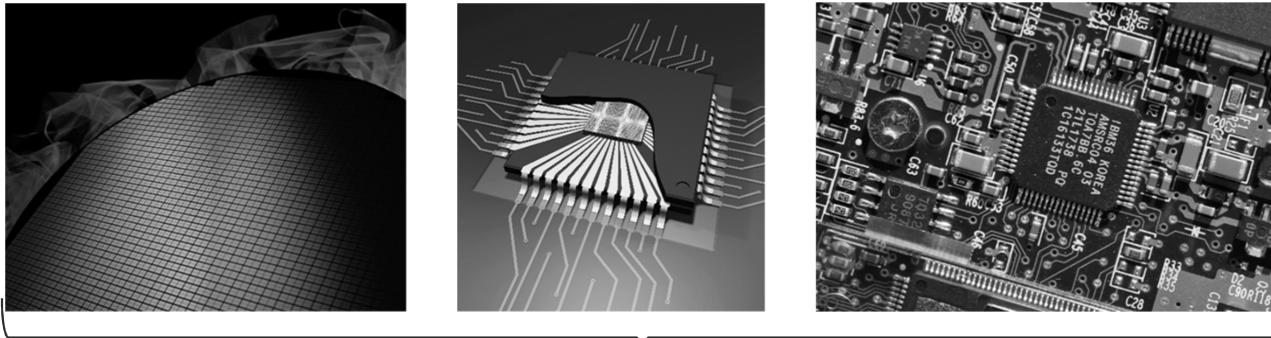

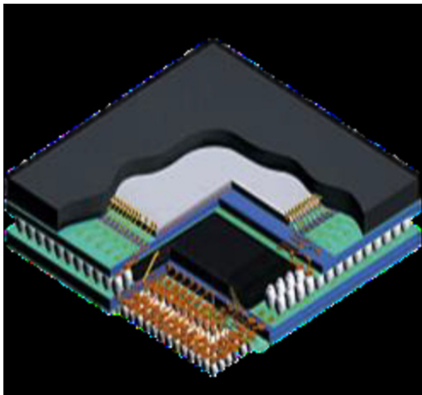

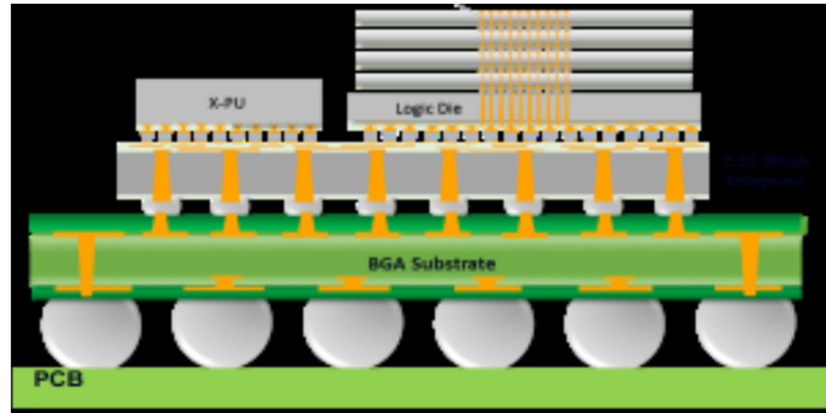

Smart Watch electronics → SIP

Smaller # of larger multichip packages

“Moore’s Law for Packaging”

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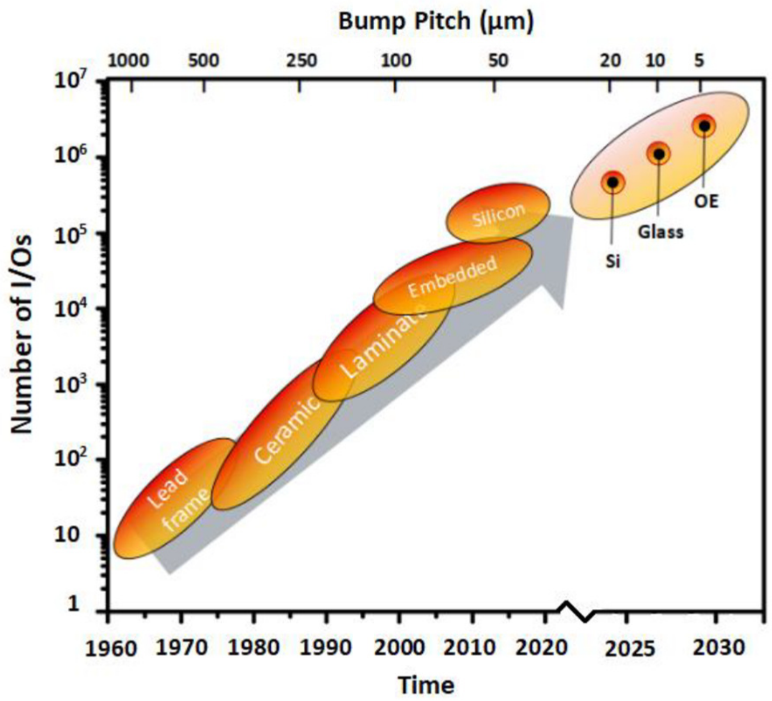

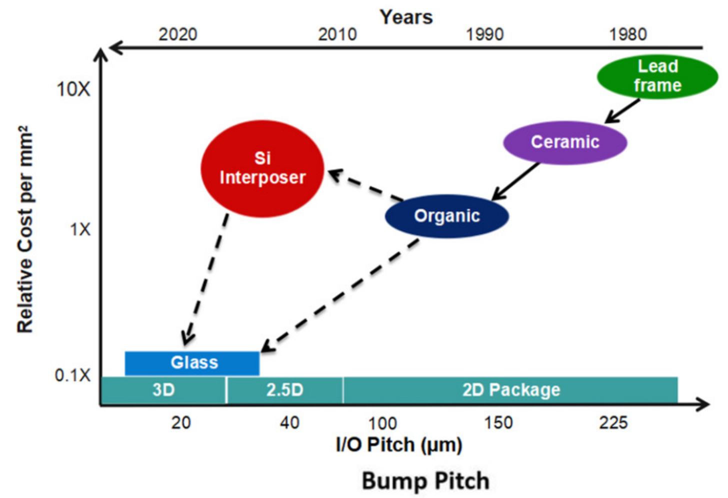

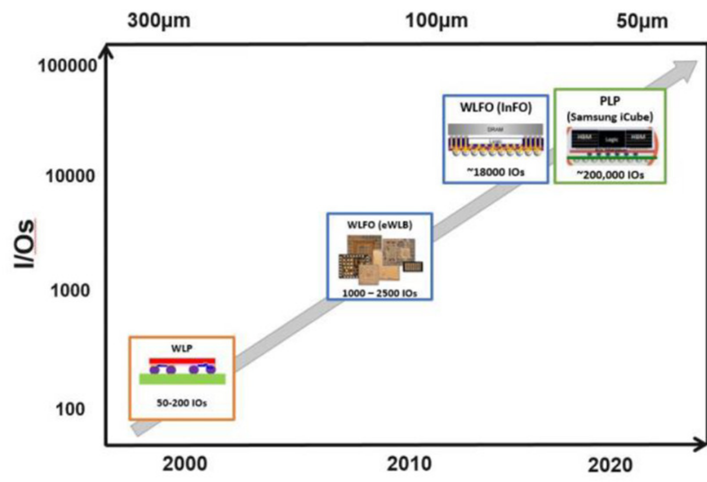

Rao Tummala, 2019 Pan Pacific Microelectronics Symposium

Factors driving package technology acceleration

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- Possible slowdown in Moore's Law shrinks
  - Integration will involve multiple chips
- Off-chip signal delays become critical
  - Logic, memory and some passives connected in same package
- More RF components, packaged closer to logic and memory
- 5G networks: new interposer materials, new designs, more filters

Feature shrinks in the package space

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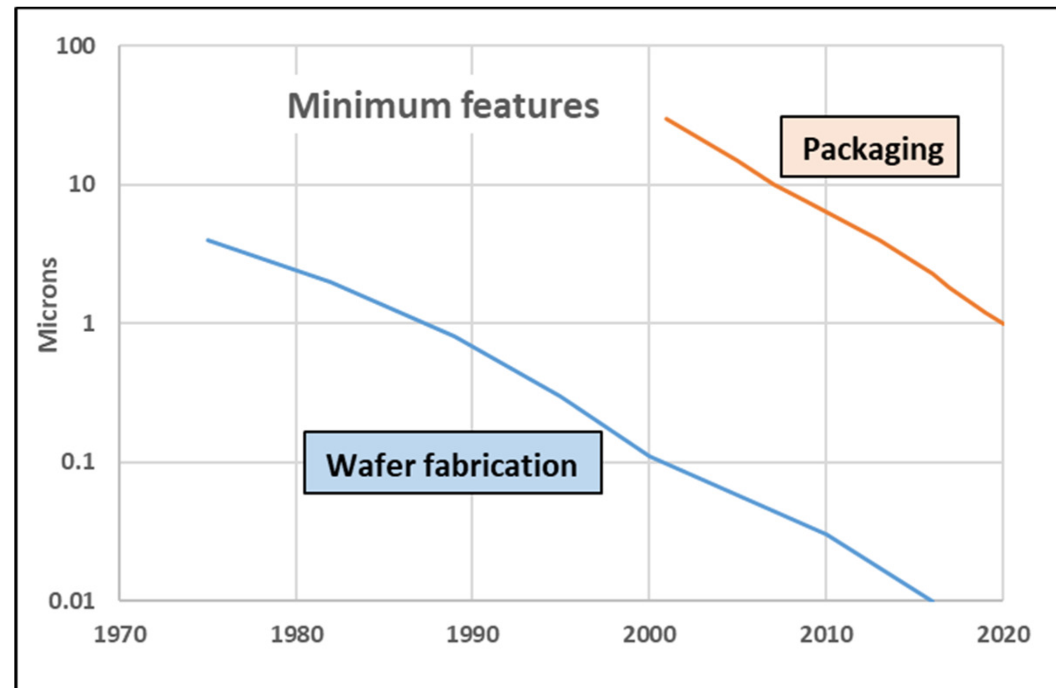
- Feature size evolution lags IC fabrication by ~ 30 years
- Entering a period of faster shrinks
- Simply dust off old semiconductor equipment and processes? No.



Unique challenges in package fabrication

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- Lithography
  - Very thick photoresists, very high aspect ratio structures: low NA lenses required
  - Challenging substrates: reconstituted wafers, panels
  - Random die placement errors: requires new alignment strategies
- PVD
  - High-outgassing substrates
  - Low stiffness substrates
  - Sensitivity to heating during process
- High temperature processes (CVD, etc) are ruled out

Metal deposition has a central role in electronics manufacturing

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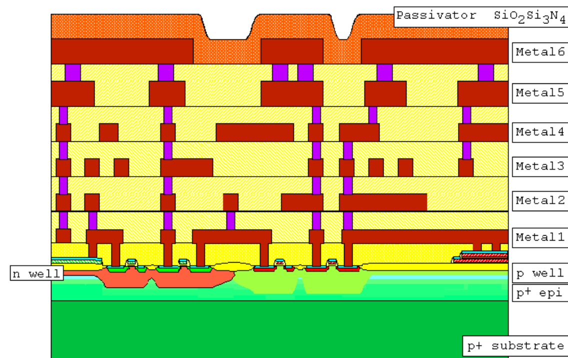
Wafer



Package

Layers of metals and insulators

Most layers are patterned

Method of metal deposition

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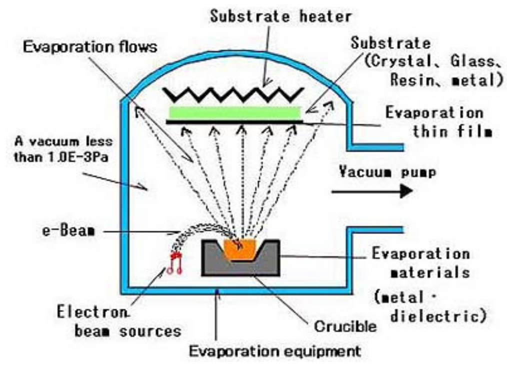
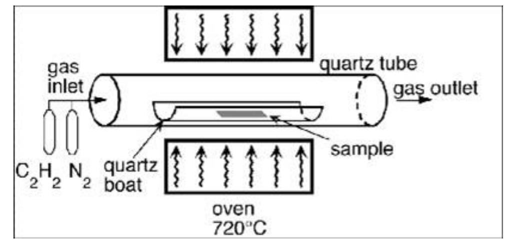
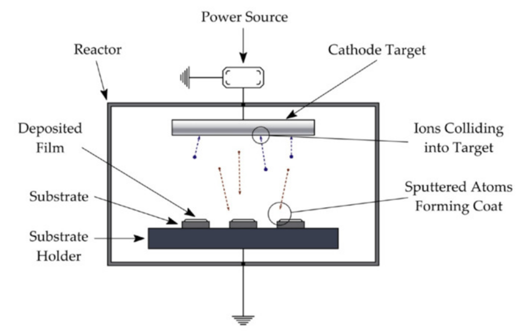
Evaporation



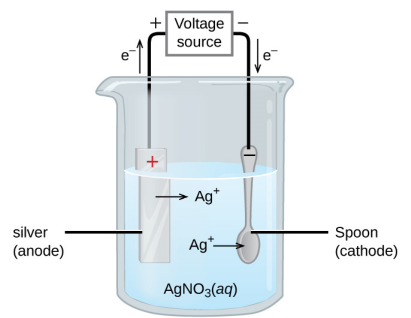
CVD



PVD



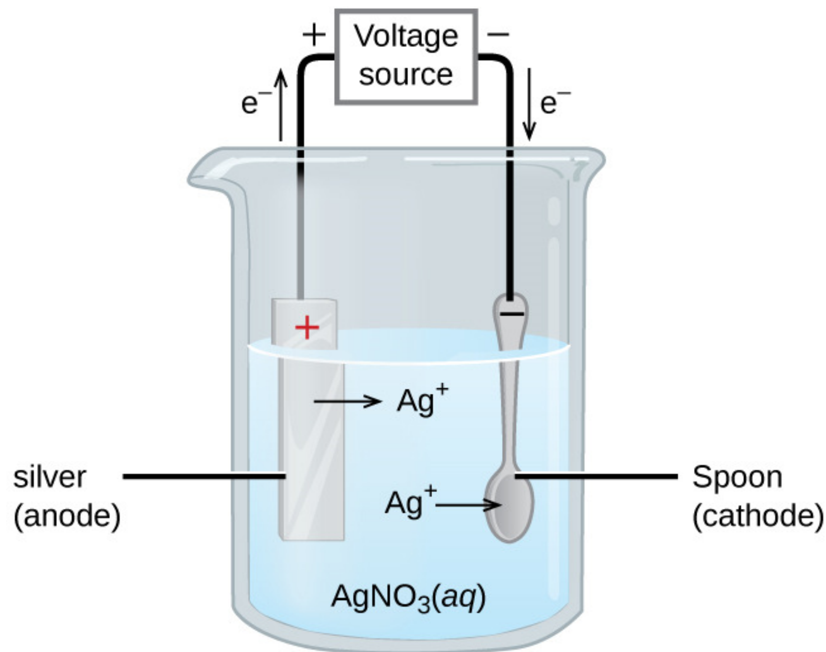
ECD (electroplating)



Others

- 3D printing
- Screen printing
- Foil lamination
- Etc

ECD (Electro Chemical Deposition)



- Components
  - Chemically resistant vessel
  - Electrolyte bath containing a metal salt
  - Anode: may or may not be the same metal as in solution
  - Cathode: substrate for deposited metal
  - Power source
- Voltage is applied between the electrodes
- Current flows across bath, carried by metal ions
- When metal ions reach the cathode surface, they are attached forming a film of solid metal

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ECD vs evaporation, CVD, PVD

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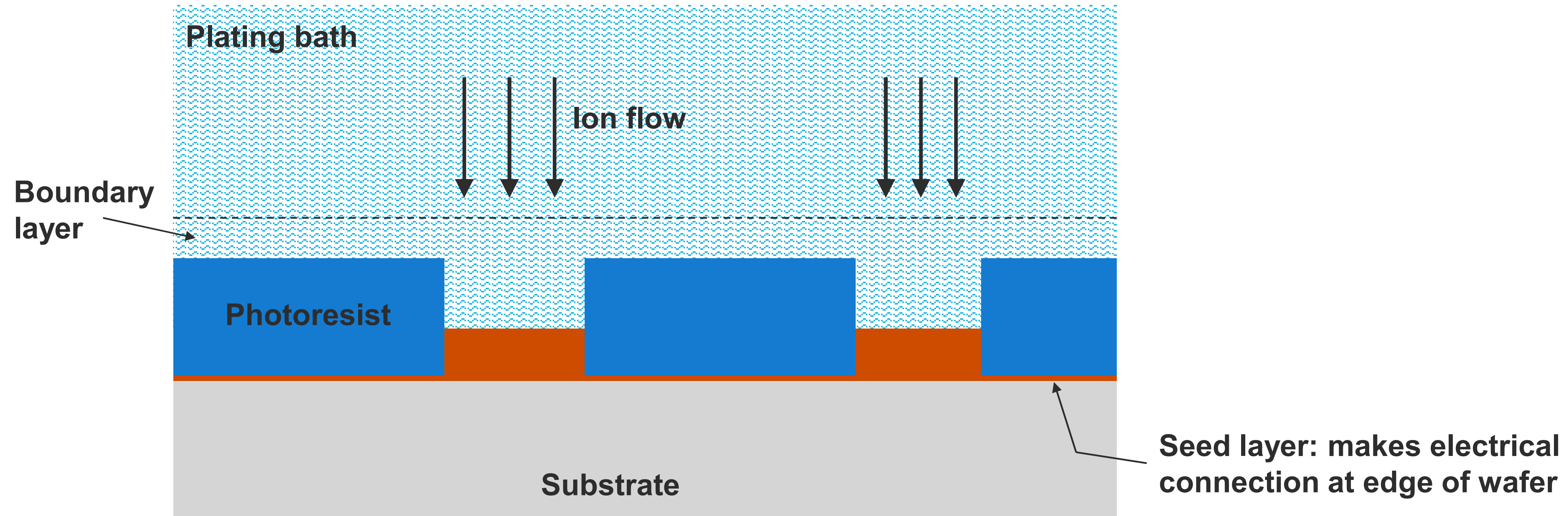
- ***Low temperature process (20 - 60 °C)***
- ***Not a vacuum process***
- ***Different set of metals available***
- ***Much faster deposition rates***
- ***Can be deposited through a photoresist pattern***
- ***Alloy deposition***
- ***Metal properties can be controlled by bath composition and process***

Patterned deposition



After plating, photoresist and seed layer are stripped

Plating in wafer fabrication

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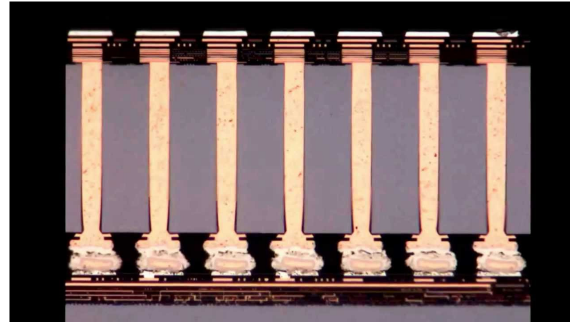
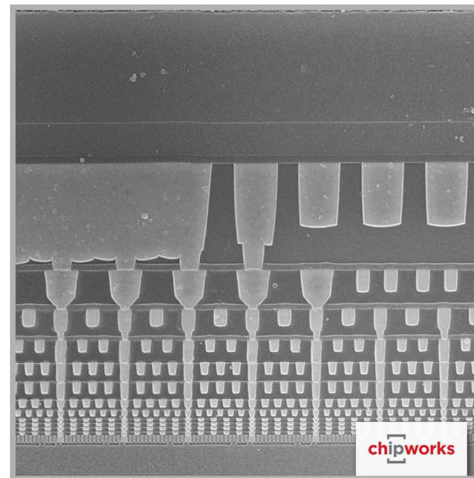
- TSV



- Damascene



Plating in device packaging

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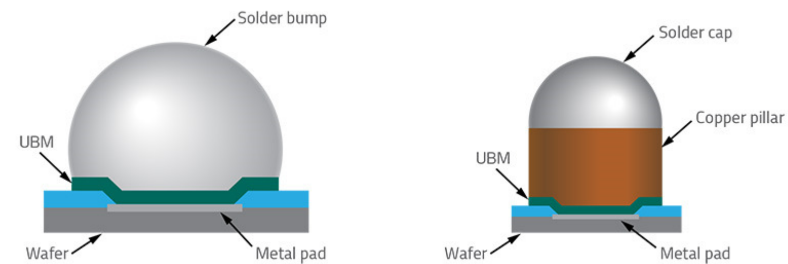
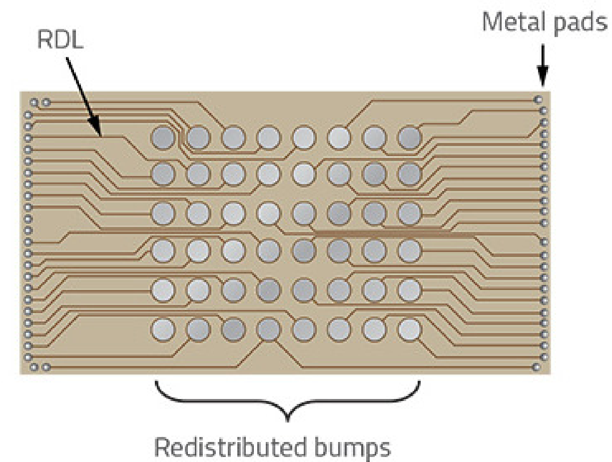
- On wafer before singulation
  - Pad buildup
  - Flip chip bumping
  - Cu pillar
  - RDL
- Other device types
  - RF filters (bond pads, inductors)
  - OE devices





Recent developments affecting plating for packaging

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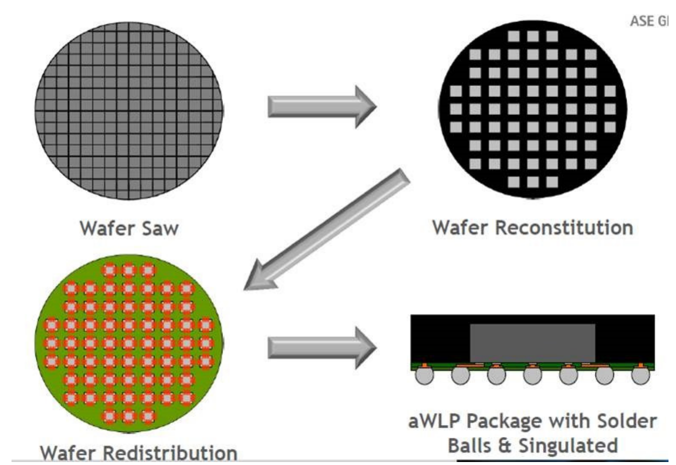
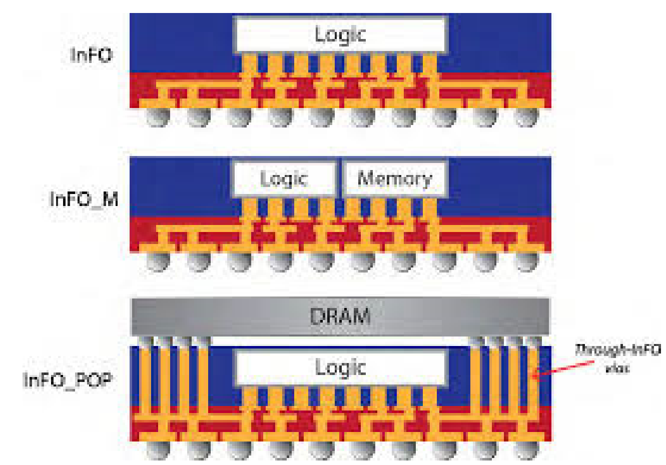
- Reconstituted wafer
- Fanout
- Interposers
- Heterogenous integration
- Panel





Challenging structures for Cu plating

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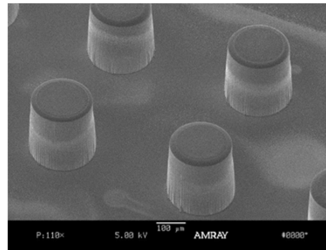
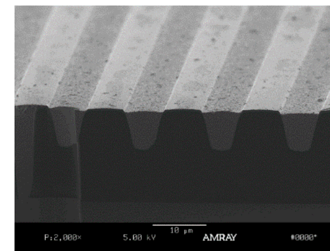
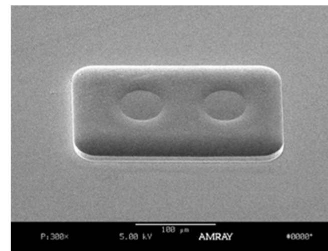
- Megapillar



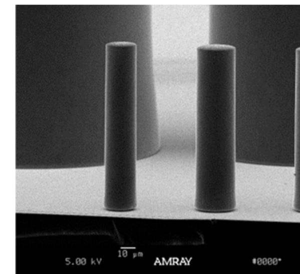
- Embedded conductor



- Large via plus pad



- 3D integrated inductor



Challenge for Cu plating: Megapillar

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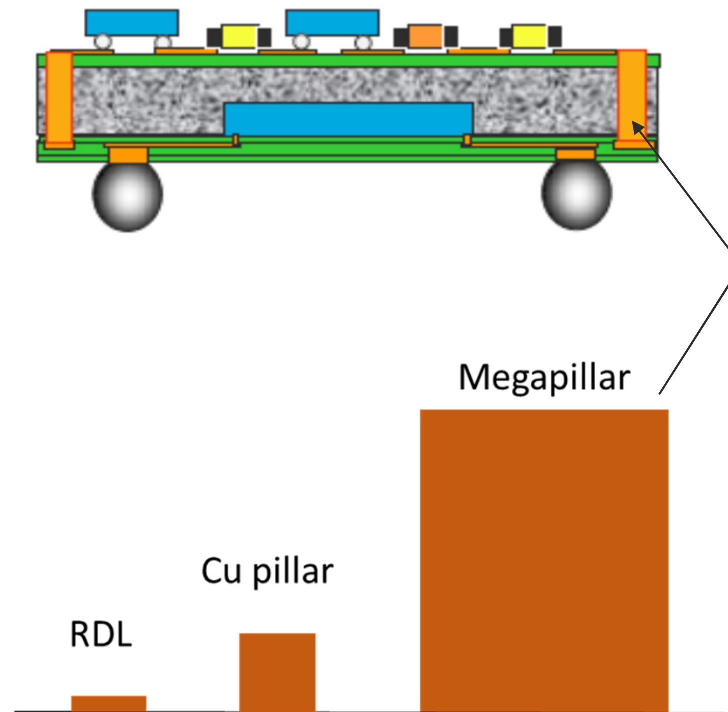
- Some fanout designs include stacking chips
- Very large Cu pillars used for power, signal and thermal conduction
- Greatly scaled-up version of Cu pillars used for chip-interposer connections



Issues in plating megapillars

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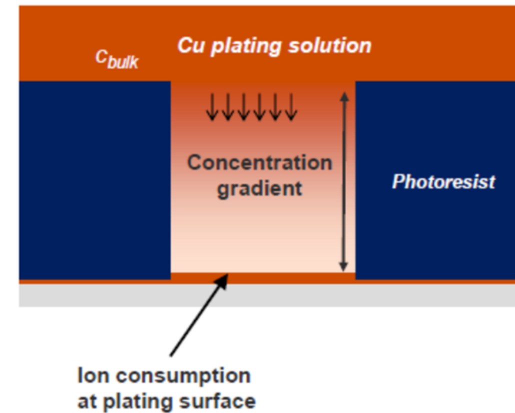
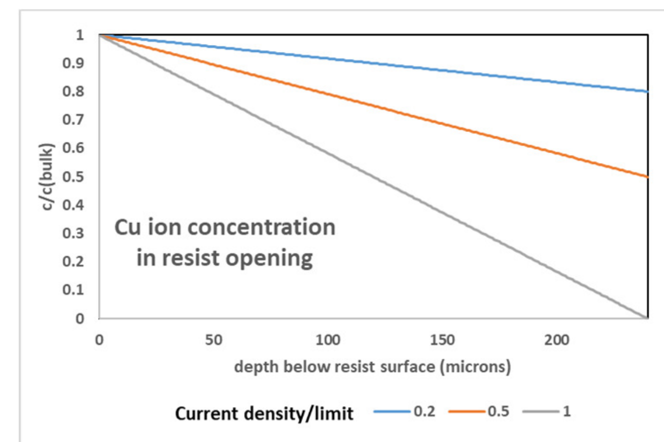
- Because of the extreme height (200μm), a high plating rate (3 to 5 μm/min) is demanded
- Because of the extreme depth of the resist feature, diffusion of Cu^{2+} ions places a strict limit on plating rate



- – **ΔV at interface drives the deposition reaction**
- – **Reaction removes Cu^{2+} ions from solution at the interface**
- – **Concentration gradient pulls Cu^{2+} ions from bulk**



Maximizing Cu diffusion

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- Steady-state diffusion:

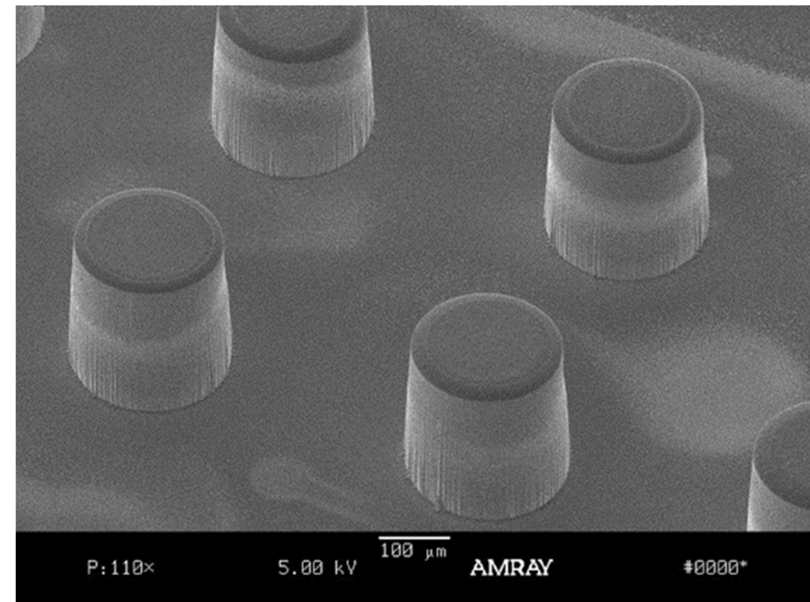
$$D\nabla^2 c = 0$$

$$j = -D\nabla c$$

- Maximum deposition rate:

$$\text{Max rate} = \varepsilon \frac{D}{\rho_{Cu}} \frac{c_{bulk}}{T_{resist}}$$

- Solution:
  - Increase D by raising bath temperature
  - Increase bulk concentration of Cu



200μm high pillars plated at 3μm/min

Embedded conductor for multilayer RDL

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- Photoresist process:
  - Conductor lines stand above dielectric
  - With multiple layers, topography stack-up presents a problem for DOF in lithography

- Embedded conductor:
  - Dielectric is patterned: photosensitive polyimide or ablation
  - Trenches are filled to create conductor lines
  - Excess metal removed by CMP

Problem: CMP may not be practical for panel substrates

Solution: modified TSV plating chemistry

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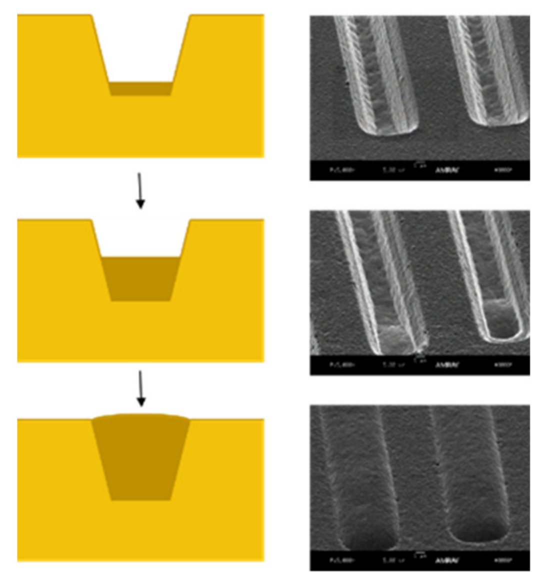
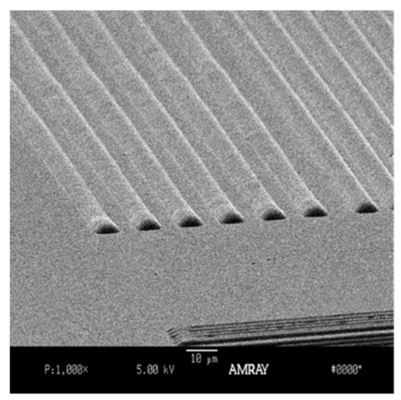
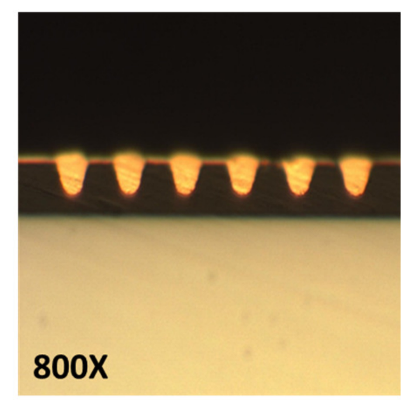
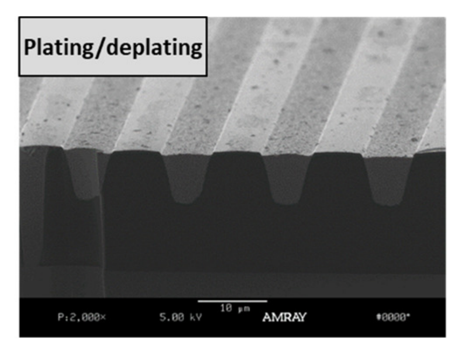
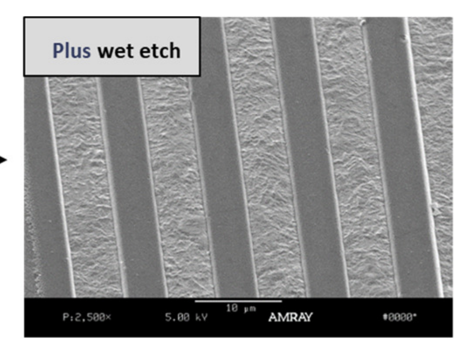
- Efficient bottom-up plating











Trenches are filled with minimal overburden, which can be stripped with deplating + wet etch

Using TSV chemistry: effect of leveler

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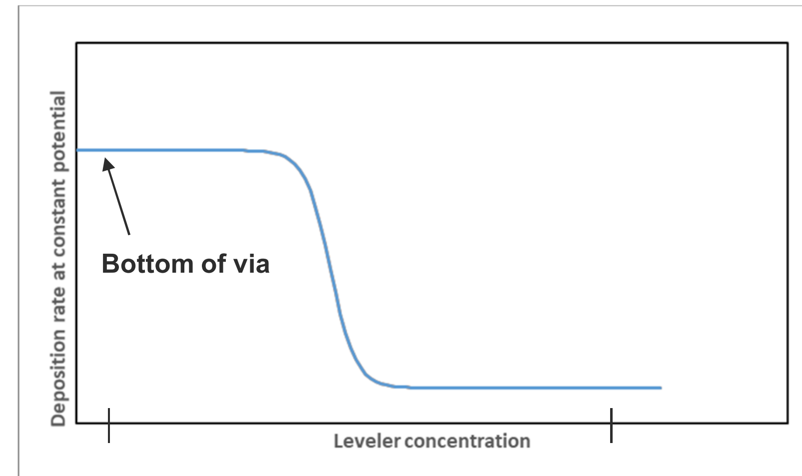
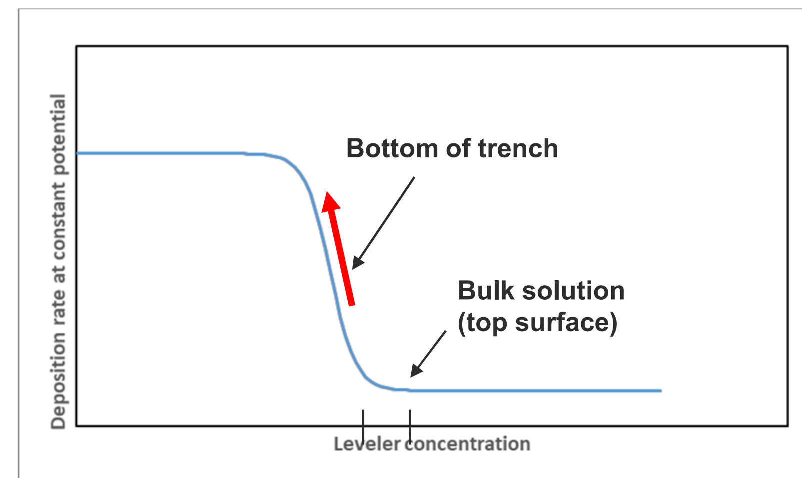
- Needed: leveler-dominated plating in one location, accelerator-dominated plating at another
- TSV:
  - Leveler is a large molecule, small diffusion coefficient
  - Very low concentration at beginning of plating, remains low throughout process
- Embedded conductor:
  - No significant separation at beginning of process
  - Geometric leveling and accelerator pileup create runaway effect at bottom of trench





Large via plus pad

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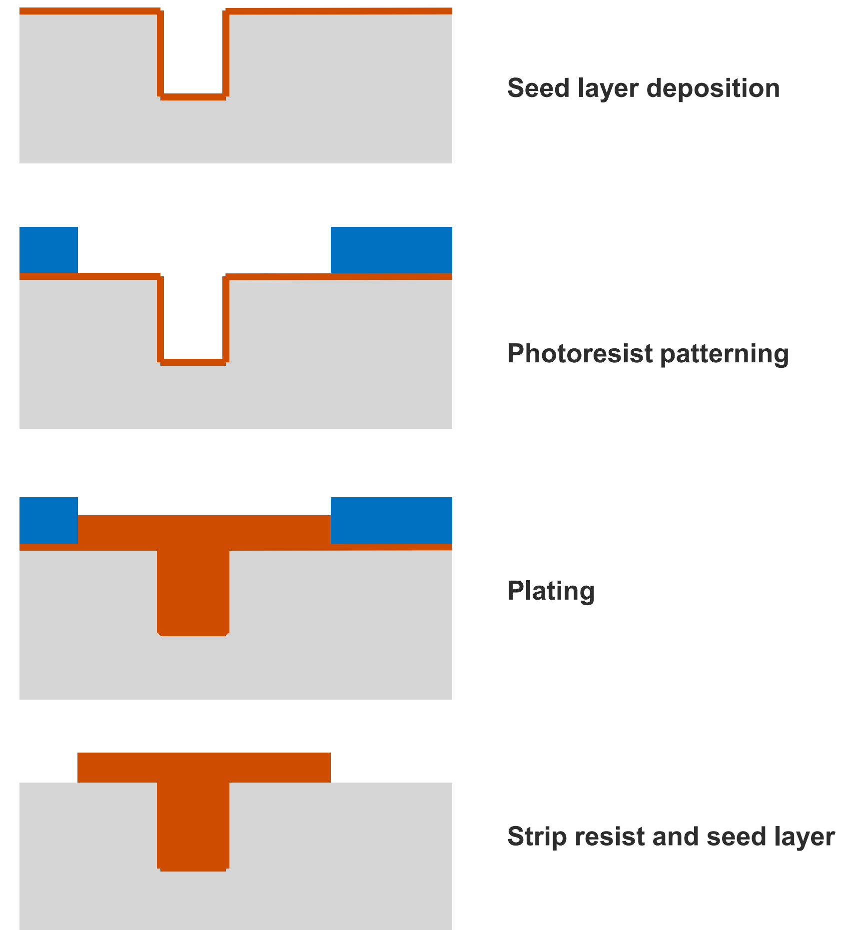
- Structure seen increasingly in RF filter and OE device applications
- Via with large dimensions: up to 70μm in depth and diameter
- Pad at the top of the via: to be plated to 5 to 20μm thickness
- Requirements:
  – Complete fill, no voids
  – Minimal dimple or mound over via
  – Flat pad, specified thickness



Problems in plating large via + pad

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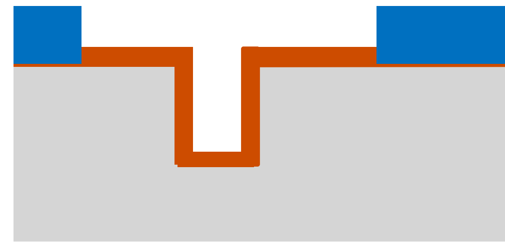
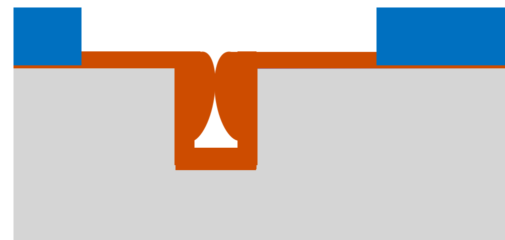
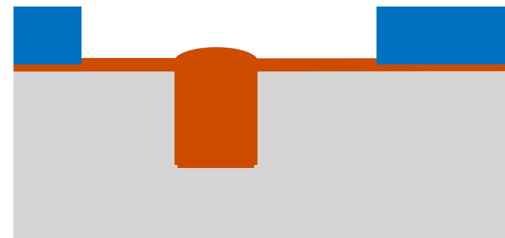
- Conformal plating: pad reaches target thickness, via not filled



- Sub-conformal: slower plating at bottom, voids form



- TSV chemistry: via fills and forms mound, pad << target thickness



Solution: less extreme leveler action

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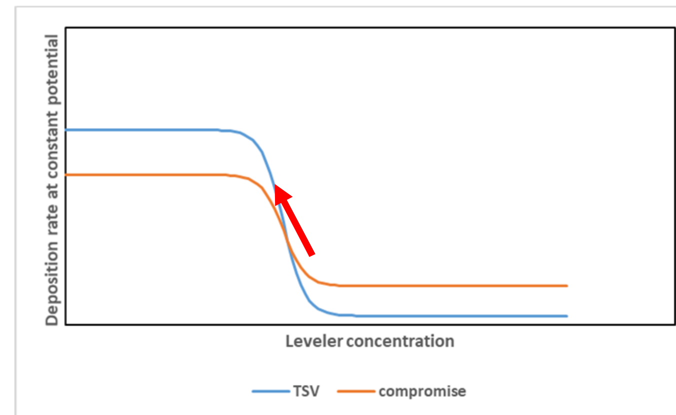
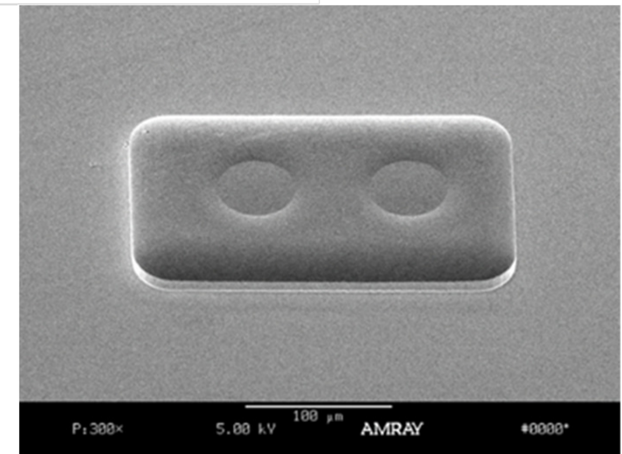
- Leveler allows higher rate at saturation
- Reduced leveler at bottom of via by combination of initial diffusion and geometric leveling
- Faster plating to fill via, but some deposition desired on pad





For arbitrary combinations of via size and pad thickness, plating + deplating may be required

Integrated 3D inductor

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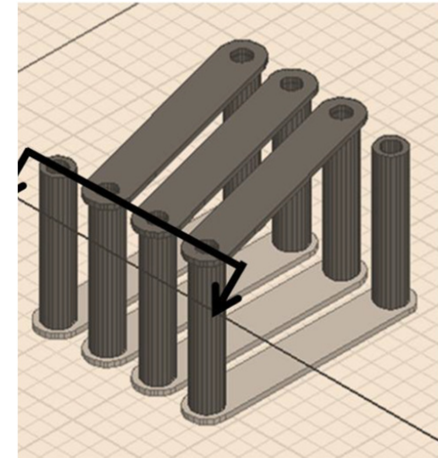
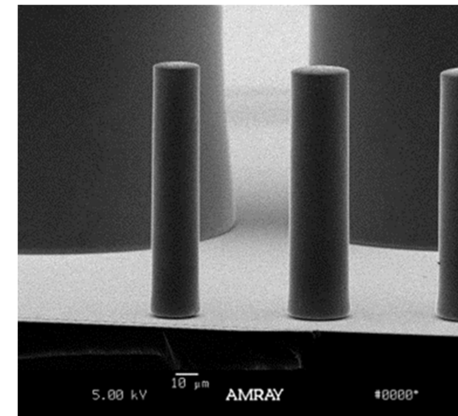
- Inductors in RF devices normally consist of flat coils
  - RDL process
- Inclusion of increasing # of filters in mobile devices creates a space crunch
- Several groups have reported on 3D design
  - Several orders of magnitude more inductance per unit area
- Requires combination of RDL (top and bottom) and high aspect ratio pillars
- Depending on dielectric, resist-defined or TSV-like process may be needed





Summary

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- Possible Moore's Law slowdown and 5G requirements are shifting technology emphasis onto the package
- ECD has a central role in this development
- Meeting the requirements for package fabrication requires innovative approaches in plating

- *The next 10 years should be very interesting!*

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Thank You

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